EXHIBIT 013

U.S. Patent No. 7,366,818 (Radulescu & Goossens)

"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Samsung Product Including Exynos System on Chip [1]
1. Integrated circuit comprising a plurality of processing modules (M, S) said modules being disposed on the same chip, and	Without conceding that the preamble of claim 1 of the '818 Patent is limiting, the Samsung Galaxy A53 (hereinafter, the "Samsung product") includes an integrated circuit. For example, the Samsung product includes the Exynos 1280 system on chip (hereinafter, the "Exynos SoC").  https://semiconductor.samsung.com/processor/showcase/smartphone/

[1] The Samsung product is charted as a representative product made used, sold, offered for sale, and/or imported by Samsung. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein

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<table>
<tr><th>'818 Patent Claim</th><th>Samsung Product Including Exynos System on Chip [1]</th></tr>
<tr><td></td><td>The Exynos SoC comprises a plurality of processing modules, for example Arm Cortex-A78 core, Cortex-A55 core, Arm Mali-G68 GPU, and AI Engine with NPU:
Specifications
<table><tr><th></th><th>Exynos 1280</th></tr><tr><td>CPU</td><td>Cortex®-A78 x 2 + Cortex®-A55 x 6</td></tr><tr><td>GPU</td><td>Mali™-G68</td></tr><tr><td>AI</td><td>AI Engine with NPU</td></tr><tr><td>Modem</td><td>5G NR Sub-6GHz 2.55Gbps (DL) / 1.28Gbps (UL)
5G NR mmWave 1.84Gbps (DL) / 0.92Gbps (UL)
LTE Cat.18 6CC 1.2Gbps (DL) / Cat.18 2CC 200Mbps (UL)</td></tr><tr><td>Connectivity</td><td>WiFi 802.11ac MIMO with Dual-band (2.4/5G),
Bluetooth® 5.2, FM Radio Rx</td></tr><tr><td>GNSS</td><td>Quad-constellation multi-signal for L1 and L5 GNSS</td></tr><tr><td>Camera</td><td>Up to 108MP in single camera mode,
Single-camera 32MP @30fps</td></tr><tr><td>Video</td><td>4K 30fps encoding and decoding</td></tr><tr><td>Display</td><td>Full HD+@120Hz</td></tr><tr><td>Memory</td><td>LPDDR4x</td></tr><tr><td>Storage</td><td>UFS v2.2</td></tr><tr><td>Process</td><td>5nm</td></tr></table>
https://semiconductor.samsung.com/resources/brochure/Exynos1280.pdf</td></tr>
<tr><td>a network (N; RN) arranged for providing at least one connection between a first and at least one second</td><td>Without conceding that the preamble of claim 1 of the '818 Patent is limiting, the Exynos SoC included in the Samsung product utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the "Arteris NoC") as a network (N; RN) arranged for providing connections between a first and at least one second module (M, S) in the Exynos SoC included in the Samsung product, wherein said modules communicate via a network on chip, either literally or under the doctrine of equivalents.</td></tr>
</table>

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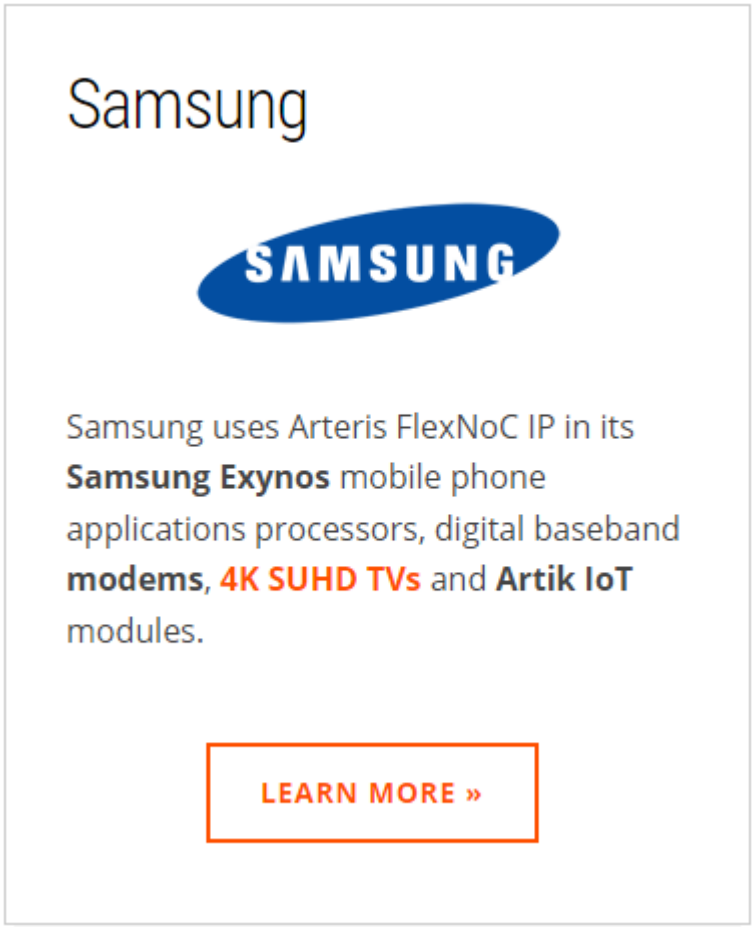
module (M, S), wherein said modules communicate via a network on chip, and	 https://web.archive.org/web/20210514110614/https://www.arteris.com/customers

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Arteris IP FlexNoC® Interconnect Licensed by Samsung's System LSI Business for Digital TV Chips

by **Kurt Shuler**, on April 23, 2019

CAMPBELL, Calif. –April 23, 2019– Arteris IP, the world's leading supplier of innovative, silicon-proven network-on-chip (NoC) interconnect semiconductor intellectual property, today announced that Samsung's System LSI Business has renewed multiple Arteris IP FlexNoC Interconnect licenses for use in multiple high-performance digital TV (DTV) processing chips utilizing Samsung's latest semiconductor technology process nodes.

> *Over many years, FlexNoC interconnect IP has helped us accelerate implementation of our digital TV chip designs on our latest semiconductor process nodes. This core interconnect technology is required to develop complex and highly optimized chips in a predictable, low-risk fashion."*

SAMSUNG

*Joeyoul Lee, Vice President, **Samsung Electronics***

Samsung first licensed FlexNoC interconnect IP in 2010. Since then, Samsung has used Arteris interconnect IP to enable complex SoC architectures in chips like the Exynos mobile processors and other electronic systems.

https://www.arteris.com/press-releases/samsung-lsi-dtv-arteris-ip-flexnoc

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Arteris Interconnect IP Solution Selected by Samsung for Mobile SoC Deployment

by **Kurt Shuler**, on November 02, 2010

Network-on-Chip (NoC) interconnect technology leader enables higher performance and more cost effective designs for mobile phone systems-on-chip (SoCs)

SUNNYVALE, California — November 2, 2010 — Arteris, Inc., a leading supplier of on-chip interconnect IP solutions, today announced that Samsung Electronics Co., Ltd., has selected Arteris' interconnect solutions for multiple chips within Samsung's mobile SOC products. Samsung chose Arteris interconnect IP to support the high speed inter-chip communication requirements in next generation mobile SOC products.

> *The Arteris interconnect IP offers us a convenient solution to handle the high speed communication needed between our SoC and external modem IC. Our customers will benefit from the lower BOM cost and power consumption as a result of this IP. We look forward to Arteris' interconnect IP helping us shorten development schedules and lower risks associated with compatibility.*

SAMSUNG

Thomas Kim, Vice President, SoC Platform Development, System LSI, ***Samsung Electronics***

https://www.arteris.com/press-releases/pr_2010_nov_02?hsLang=en-us

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	For example, in the Arteris NoC, "[m]ost transactions require the following two-step transfers," including "[a] master send[ing] request packets" and "the slave return[ing] response packets": ***11.3.1.1 Transaction Layer*** The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets

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	on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.

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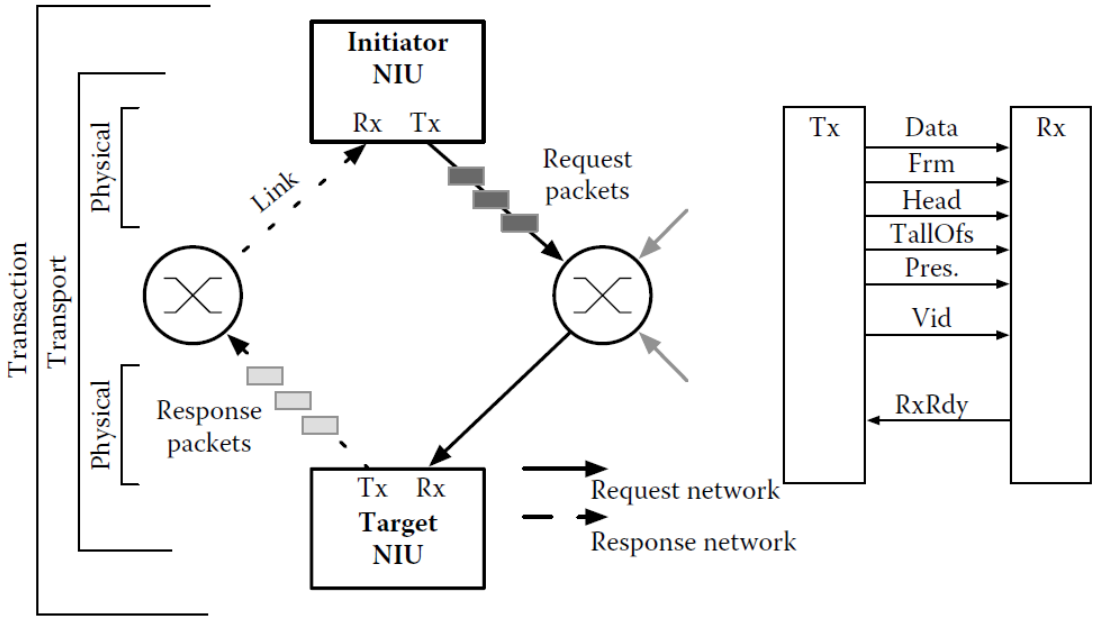

FIGURE 11.1
NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.

See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313; *see id* at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: "In this chapter we will present an MPSoC platform […] using Arteris NoC as communication infrastructure.").

A large SoC, such as the Exynos SoC included in the Samsung product may include multiple classes of Arteris NoC:

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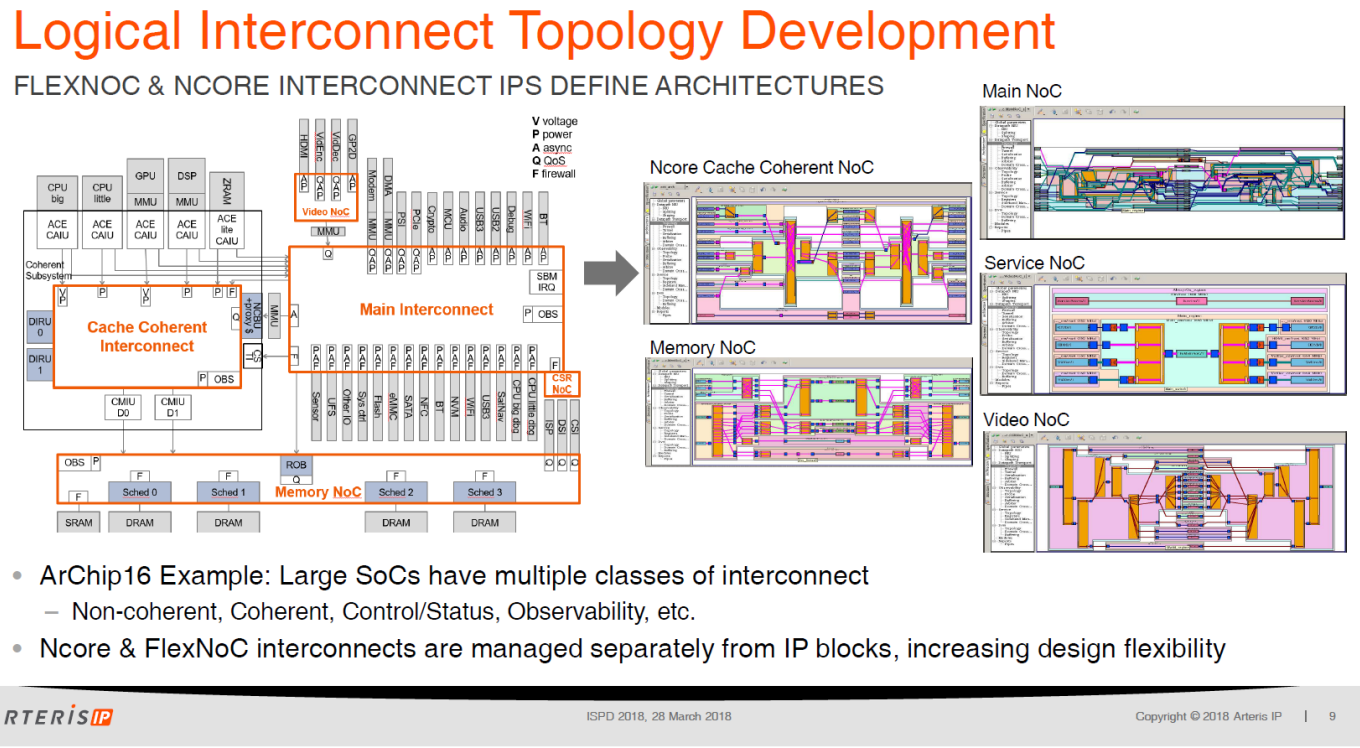

See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.

As a further illustration, connections between modules within the Arteris NoC may be defined by a connectivity table:

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	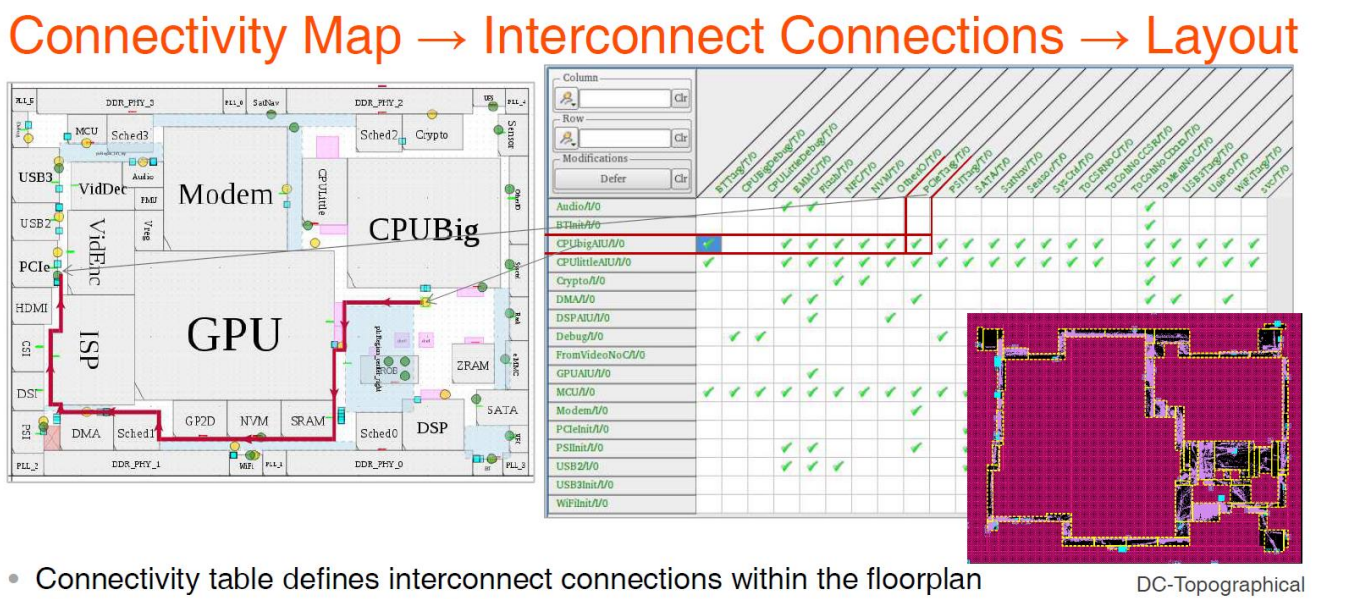 *See* Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12.
wherein said connection supports transactions comprising outgoing messages	The Arteris NoC utilized by the Exynos SoC included in the Samsung product has a connection that supports transactions comprising outgoing messages from the first module to the second modules and return messages from the second modules to the first module, either literally or under the doctrine of equivalents. For example, in the Arteris NoC, "[m]ost transactions require the following two-step transfers," including "[a] master send[ing] request packets" and "the slave return[ing] response packets":

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from the first module to the second modules and return messages from the second modules to the first module	***11.3.1.1 Transaction Layer*** The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.

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	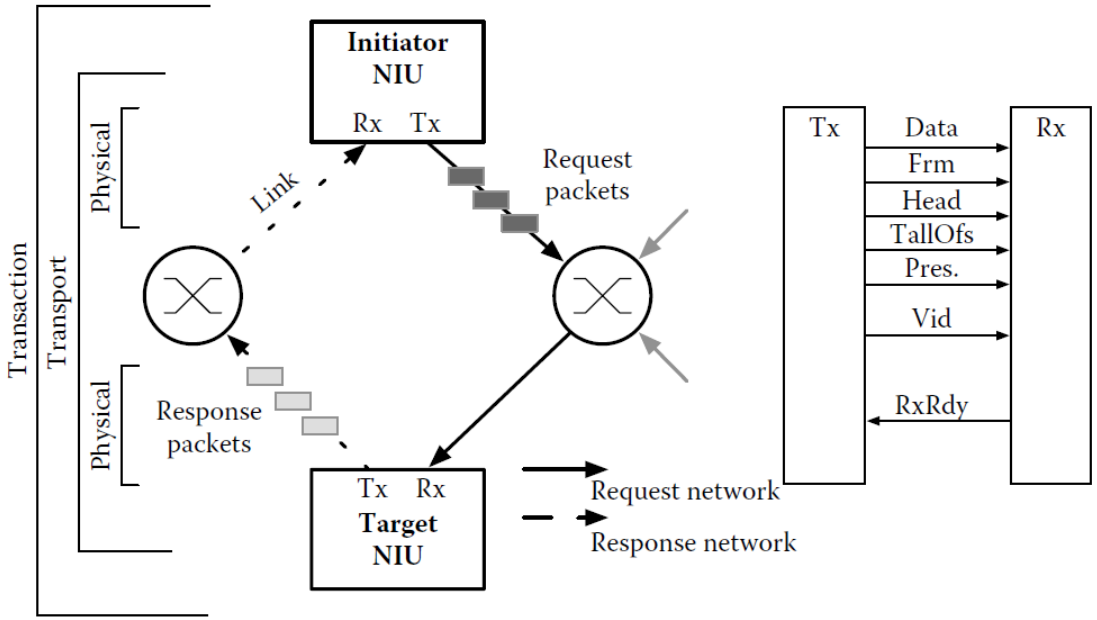 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.
the integrated circuit comprising at least one dropping means (DM) for dropping	The Arteris NoC utilized by the Exynos SoC included in the Samsung product has at least one dropping means (DM) for dropping data exchanged by said first and second module (M, S), either literally or under the doctrine of equivalents.

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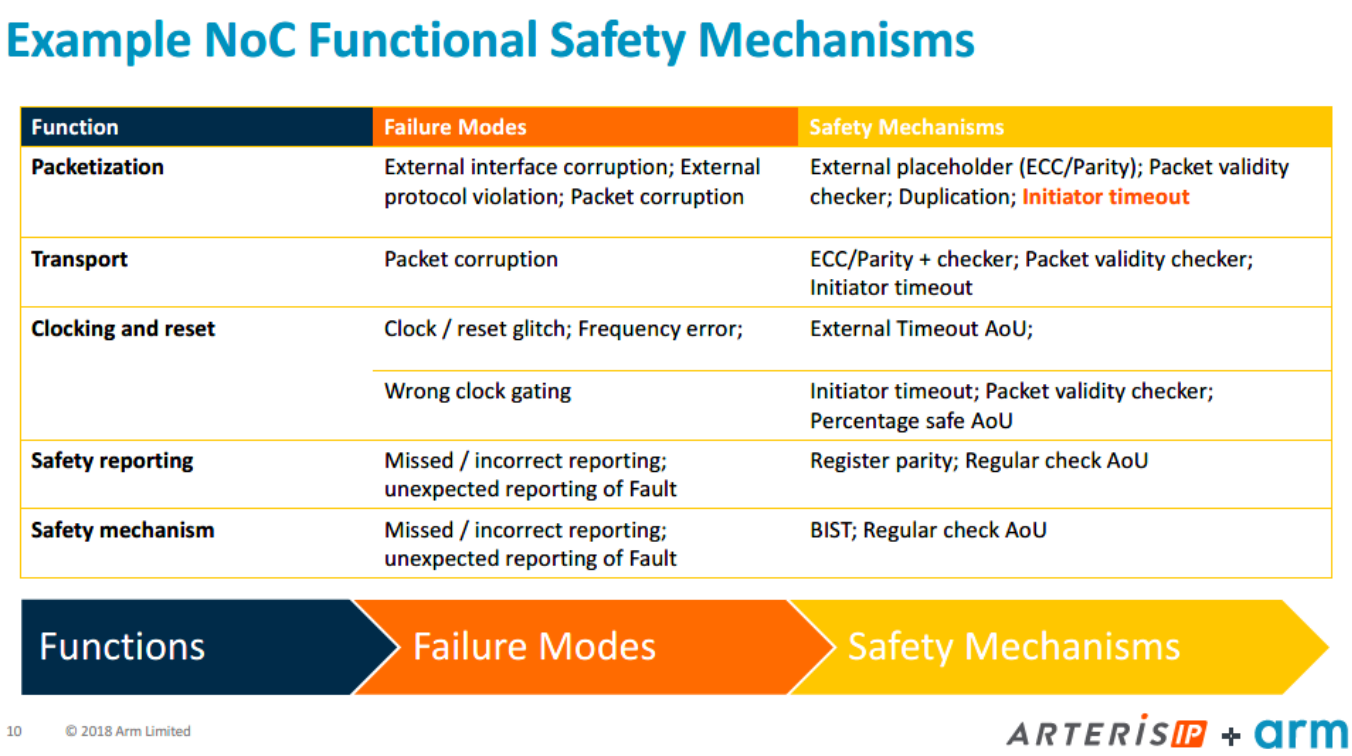
data exchanged by said first and second module (M, S), and	For example, the Arteris NoC addresses packet corruption using, among other mechanisms, "packet validity checker" and "initiator timeout," which may result in data being dropped:



Implementing ISO 26262 Compliant AI Systems with Arm and Arteris IP, https://www.arteris.com/download-arm-arteris-ip-ai-npu-iso26262-presentation, at 10.

As a further example, the Arteris NoC includes "packet validity checking" and "transaction timeout" for error resiliency, which may result in data being dropped:

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	A. Advanced Data Protection and Reliability for SoC Interconnects Arteris FlexNoC expands data protection and reliability features beyond the CPU and into the network-on-chip interconnect fabric. [14] FlexNoC can pass IP-generated error-correcting code (ECC) information through the NoC between socket interfaces. Alternatively, FlexNoC can generate custom data payload and control ECC in packet-generating units, and detect or correct errors in packet-consuming units. The amount of redundancy per data byte is configurable based on the cost and resilience requirements of the SSD controller. The FlexNoC Resilience package also includes packet validity checking, transaction timeout, control register parity checking and unit duplication and comparison that are all designed to extend error resiliency beyond the CPU and into the other hardware blocks of the design. Key to a complete implementation is the inclusion of a safety controller to manage faults and a fully-verified built-in test (BIST) module to continually test data protection hardware when activity is quiescent. Optimizing Enterprise-Class SSD Host Controller Design with Arteris FlexNoC Network-On-Chip Interconnect IP, https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf at 7. As a further example, in the Arteris NoC, "[t]arget-side timeout in the network interface units detects unresponsive target IP failures and ensures that they do not block the NoC," which may result in data being dropped:

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	C. Transaction Timeout Target-side timeout in network interface units detects unresponsive target IP failures and ensures that they do not block the NoC. Initiator-side timeout in network interface units detects transport packet deletion, bad routing, or failures of stuck arbiters or targets. Timeout is detected per transaction using a pre-scaled counter to minimized hardware cost and power consumption. SoC Reliability Features in the FlexNoC Resilience Package, http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf at 2.
at least one interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN),	The Arteris NoC utilized by the Exynos SoC included in the Samsung product has at least one interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN), either literally or under the doctrine of equivalents. For example, the Arteris NoC uses Network Interface Units (NIUs), which "translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols" and in the Arteris NoC, the NIUs "are at the boundary of the NoC" and there is a NIU connected to each of the master and slave nodes, between the nodes and the network:

'818 Patent Claim	Samsung Product Including Exynos System on Chip [1]
	11.3.1.1 Transaction Layer The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.

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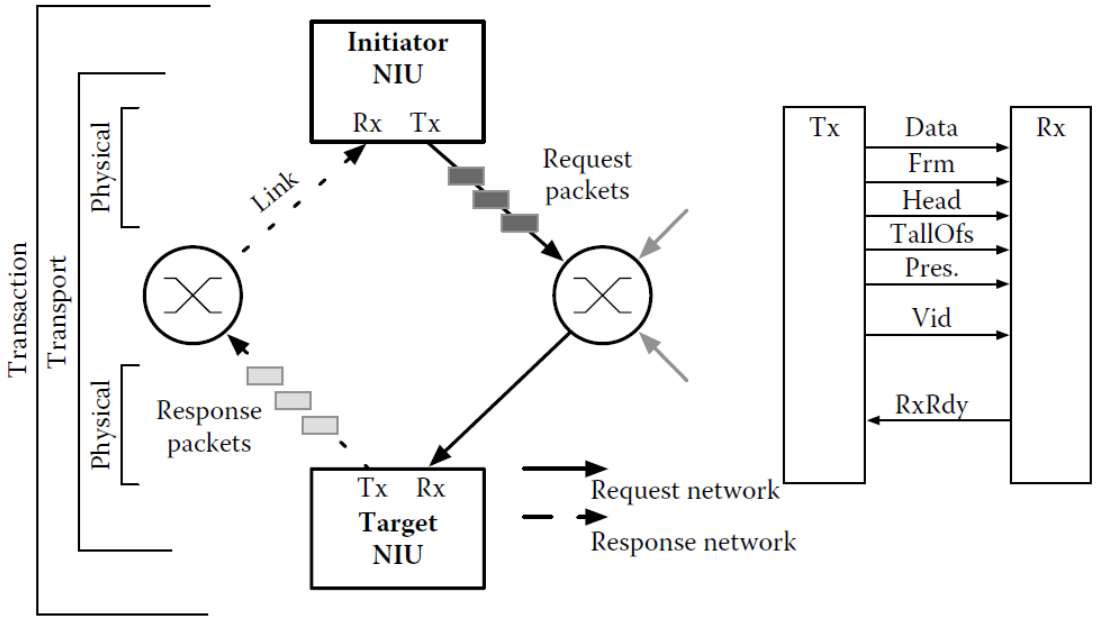

FIGURE 11.1
NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.

See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313.

The Initiator NIUs are "used to connect a master node to the NoC," and the Target NIUs are "used to connect a slave node to the NoC":

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	11.3.2 Network Interface Units The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated: • **Initiator NIU**—third party protocol-to-NTTP, used to connect a master node to the NoC • **Target NIUs**—NTTP-to-third party protocol, used to connect a slave node to the NoC Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317. In the Arteris NoC "Initiator NIU units…enable connection between an AMBA-AHB master IP and the NoC":

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	11.3.2.1 Initiator NIU Units Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU. A FIFO memory is inserted in the datapath for AHB write accesses. The FIFO memory absorbs data at the AHB initiator rate, so that NTTP packets can

'818 Patent Claim	Samsung Product Including Exynos System on Chip [1]
	burst at NoC rate as soon as a minimum amount of data has been received. The width of the FIFO and the AHB data bus is identical, and the FIFO depth is defined by the hardware parameter. This parameter indicates the amount of data required to generate a Store packet: each time the FIFO is full, a Request packet is sent on the Tx port. Of course, if the AHB access ends before the FIFO is full, the NTTP request packet is sent. Because AHB can only tolerate a single outstanding transaction, the AHB bus is frozen until the NTTP transaction has been completed. That is • During a read request, until the requested data arrives from the Rx port • During a nonbufferable write request, in which case only the last access is frozen and the acknowledge occurs when the last NTTP response packet has been received • When an internal FIFO is full

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NIU Architecture

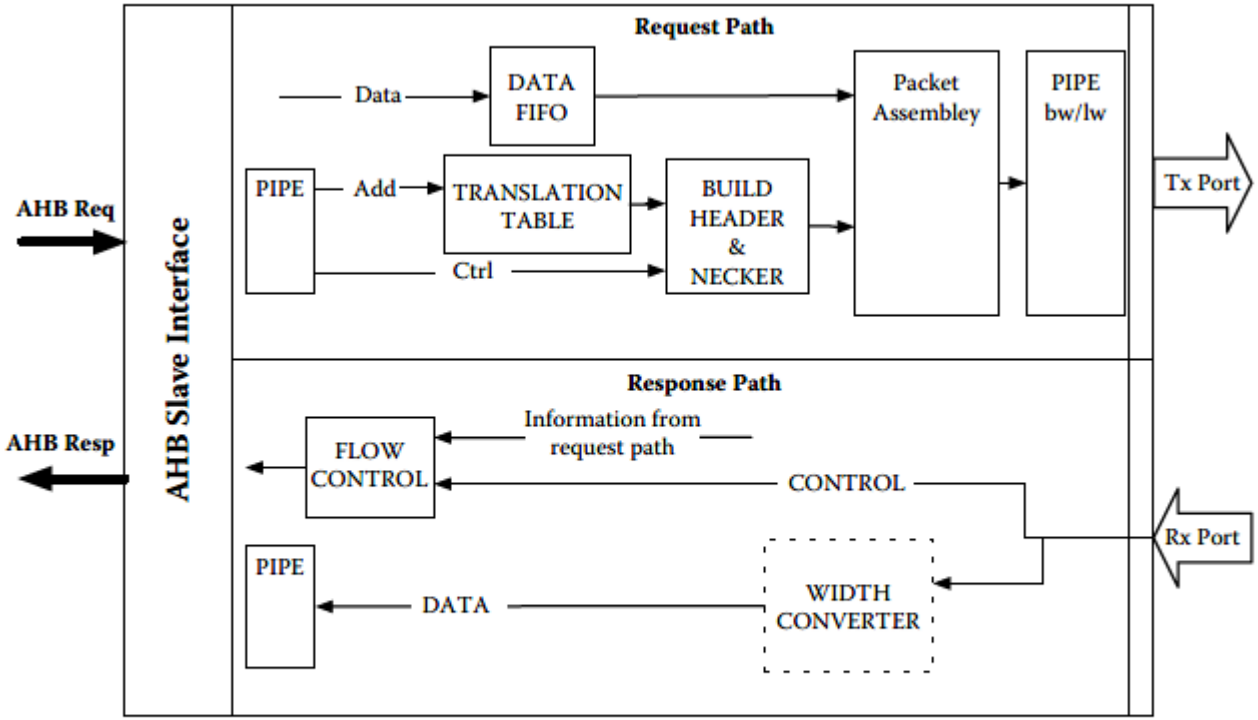

FIGURE 11.4
Network interface unit: Initiator architecture.

Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317-318.

As further example, "Target NIU units enable connection of a slave IP to the NoC by translating

'818 Patent Claim	Samsung Product Including Exynos System on Chip [1]
	NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets": ***11.3.2.2 Target NIU Units*** Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always 32 bits wide, but the actual address space size may be downsized by setting a hardware parameter. Unused AHB address bits are then driven to zero. The NTTP request packet is then translated into one or more corresponding AHB accesses, depending on the transaction type (word aligned or nonaligned access). For example, if the request is an atomic Store, or a Load that can fit an AHB burst of specified length, then such a burst is generated. Otherwise, an AHB burst with unspecified length is generated.

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Target NIU Architecture

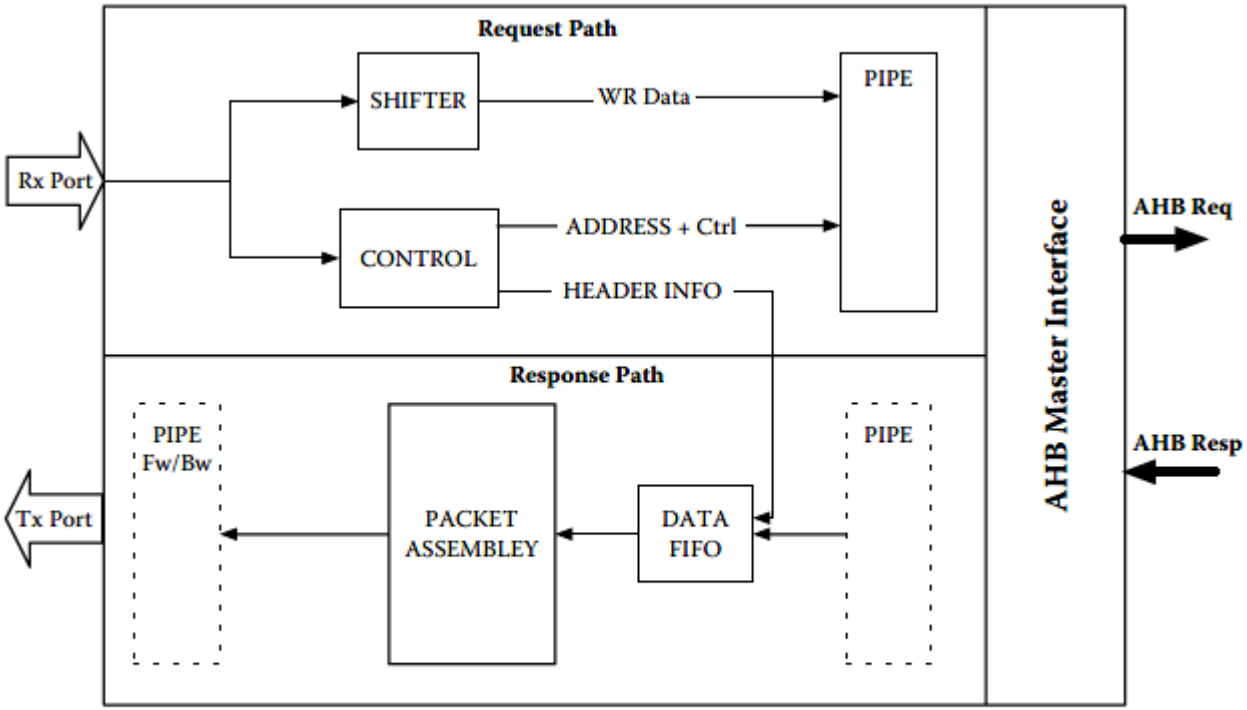

FIGURE 11.5
Network interface unit: Target architecture.

Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 318-319.

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wherein said interface means (ANIP, PNIP) comprises a first dropping means (DM) for dropping data, and	The interface means of the Arteris NoC utilized by the Exynos SoC included in the Samsung product comprises a first dropping means (DM) for dropping data, either literally or under the doctrine of equivalents. For example, the Arteris NoC uses Network Interface Units (NIUs), which include Initiator NIUs, that are "used to connect a master node to the NoC," and the Target NIUs, that are "used to connect a slave node to the NoC": **11.3.2 Network Interface Units** The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated: • **Initiator NIU**—third party protocol-to-NTTP, used to connect a master node to the NoC • **Target NIUs**—NTTP-to-third party protocol, used to connect a slave node to the NoC Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317. For example, the Arteris NoC addresses packet corruption using, among other mechanisms, "packet validity checker" and "initiator timeout," which may result in data being dropped:

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Example NoC Functional Safety Mechanisms

Function	Failure Modes	Safety Mechanisms
Packetization	External interface corruption; External protocol violation; Packet corruption	External placeholder (ECC/Parity); Packet validity checker; Duplication; **Initiator timeout**
Transport	Packet corruption	ECC/Parity + checker; Packet validity checker; Initiator timeout
Clocking and reset	Clock / reset glitch; Frequency error;	External Timeout AoU;
	Wrong clock gating	Initiator timeout; Packet validity checker; Percentage safe AoU
Safety reporting	Missed / incorrect reporting; unexpected reporting of Fault	Register parity; Regular check AoU
Safety mechanism	Missed / incorrect reporting; unexpected reporting of Fault	BIST; Regular check AoU

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Implementing ISO 26262 Compliant AI Systems with Arm and Arteris IP, https://www.arteris.com/download-arm-arteris-ip-ai-npu-iso26262-presentation, at 10.

As a further example, the Arteris NoC "can pass IP-generated error-correcting code (ECC) information through the NoC between the socket interfaces" and includes "packet validity checking" and "transaction timeout" for error resiliency, which may result in data being dropped:

U.S. Patent No. 7,366,818 (Radulescu & Goossens)
"Integrated circuit comprising a plurality of processing modules and a network and method for exchanging data using same"

'818 Patent Claim	Samsung Product Including Exynos System on Chip [1]
	A. Advanced Data Protection and Reliability for SoC Interconnects Arteris FlexNoC expands data protection and reliability features beyond the CPU and into the network-on-chip interconnect fabric. [14] FlexNoC can pass IP-generated error-correcting code (ECC) information through the NoC between socket interfaces. Alternatively, FlexNoC can generate custom data payload and control ECC in packet-generating units, and detect or correct errors in packet-consuming units. The amount of redundancy per data byte is configurable based on the cost and resilience requirements of the SSD controller. The FlexNoC Resilience package also includes packet validity checking, transaction timeout, control register parity checking and unit duplication and comparison that are all designed to extend error resiliency beyond the CPU and into the other hardware blocks of the design. Key to a complete implementation is the inclusion of a safety controller to manage faults and a fully-verified built-in test (BIST) module to continually test data protection hardware when activity is quiescent. Optimizing Enterprise-Class SSD Host Controller Design with Arteris FlexNoC Network-On-Chip Interconnect IP, https://www.arteris.com/hubfs/enterprise-ssd-controller-tech-paper-arteris.pdf at 7. As a further example, in the Arteris NoC, "[t]arget-side timeout in the network interface units detects unresponsive target IP failures and ensures that they do not block the NoC," which may result in data being dropped:

'818 Patent Claim	Samsung Product Including Exynos System on Chip [1]
	C. Transaction Timeout Target-side timeout in network interface units detects unresponsive target IP failures and ensures that they do not block the NoC. Initiator-side timeout in network interface units detects transport packet deletion, bad routing, or failures of stuck arbiters or targets. Timeout is detected per transaction using a pre-scaled counter to minimized hardware cost and power consumption. SoC Reliability Features in the FlexNoC Resilience Package, http://itersnews.com/wp-content/uploads/experts/2015/03/95935flexnoc-resilience-package-tech-paper.pdf at 2.
wherein the dropping of data and therefore the transaction completion can be controlled by the interface means.	In the Arteris NoC utilized by the Exynos SoC included in the Samsung product, the transaction completion can be controlled by the interface means, either literally or under the doctrine of equivalents. For example, the Arteris NoC uses Network Interface Units (NIUs), which include Initiator NIUs, that are "used to connect a master node to the NoC," and the Target NIUs, that are "used to connect a slave node to the NoC": **11.3.2 Network Interface Units** The Arteris Danube IP library includes NIUs for different third party protocols. Currently, three different protocols are supported: AHB (APB), OCP, and AXI. For each protocol, two different NIU units can be instantiated:

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	• **Initiator NIU**—third party protocol-to-NTTP, used to connect a master node to the NoC • **Target NIUs**—NTTP-to-third party protocol, used to connect a slave node to the NoC Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 316-317. For example, the Arteris NoC addresses packet corruption using, among other mechanisms, "packet validity checker" and "initiator timeout," which may result in data being dropped:

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Example NoC Functional Safety Mechanisms

Function	Failure Modes	Safety Mechanisms
Packetization	External interface corruption; External protocol violation; Packet corruption	External placeholder (ECC/Parity); Packet validity checker; Duplication; **Initiator timeout**
Transport	Packet corruption	ECC/Parity + checker; Packet validity checker; Initiator timeout
Clocking and reset	Clock / reset glitch; Frequency error;	External Timeout AoU;
	Wrong clock gating	Initiator timeout; Packet validity checker; Percentage safe AoU
Safety reporting	Missed / incorrect reporting; unexpected reporting of Fault	Register parity; Regular check AoU
Safety mechanism	Missed / incorrect reporting; unexpected reporting of Fault	BIST; Regular check AoU

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